

Feature

- Chips are electrically insulated from plate
- Package in compliance with international standard. Pressure type, excellent temperature characteristics and power cycling capability
- 350A below modules are forced air cooling, 400A above modules can be selected by air cooling or water cooling

| | |
|-------------------|------------------|
| $I_{T(AV)}$ | 1000A |
| V_{DRM}/V_{RRM} | 100-6500V |
| I_{TSM} | 20 KA |
| I^2t | 2000 $10^3 a^2s$ |

Typical application

- AC, DC motor control, Different kind of rectifying power supply
- Industrial heating and control, Light adjustment, Non-contact switch
- Motor softstarter, Static reactive power compensation
- Welding equipment, Frequency transformer, UPS, Battery charging and discharging

| SYMBOL | CHARACTERISTIC | TEST CONDITIONS | T_J (°C) | VALUE | | UNIT |
|------------------------|--|--|---------------|-------|-------|---------------|
| | | | | Min | Max | |
| $I_{T(AV)}$ | Mean on-state current | 180° half sine wave, 50HZ Double side cooled, $T_C=98^\circ C$ | 125 | | 1000 | A |
| $I_{T(RMS)}$ | RMS current | | 125 | | 1570 | A |
| V_{DRM} V_{RRM} | Repetitive peak off-state voltage Repetitive peak reverse voltage | $V_{DRM} \& V_{RRM} tp=10ms$ $V_{DSM} \& V_{RSM} = V_{DRM} \& V_{RRM} + 200V$ | 125 | 500 | 2500 | V |
| I_{DRM} I_{RRM} | Repetitive peak current | $V_{DM} = V_{DRM}$ $V_{RM} = V_{RRM}$ | 125 | | 50 | mA |
| I_{TSM} | Surge on-state current | 10ms half sine wave | 125 | | 20.0 | KA |
| I^2t | I^2t for fusing coordination | $V_R = 0.6V_{RRM}$ | | | 2000 | $A^{2S} * 10$ |
| V_{TO} | Threshold voltage | | 125 | | 0.80 | V |
| r_T | On-state slope resistance | | | | 0.33 | mΩ |
| V_{TM} | Peak on-state voltage | $I_{TM} = 3000A$ | 25 | | 1.20 | V |
| dv/dt | Critical rate of rise of off-state voltage | $V_{DM} = 0.67V_{DRM}$ | 125 | | 800 | V/us |
| di/dt | Critical rate of rise of on-state current | $V_{DM} = 67\% V_{DRM}$ TO 1000A, Gate pulse $tr \leq 0.5us$ $I_{GM} = 1.5A$ | 125 | | 100 | A/us |
| I_{GT} | Gate trigger current | $V_A = 12V, I_A = 1A$ | 25 | 30 | 200 | mA |
| V_{GT} | Gate trigger voltage | | | 0.8 | 3 | V |
| I_H | Holding current | | | 20 | 200 | mA |
| V_{GD} | Npn-trigger gate voltage | $V_{DM} = 0.67V_{DRM}$ | 125 | | 0.2 | V |
| $R_{th(j-c)}$ | Thermal impedance node to the shell | 180° sine wave, single heat sink | | | 0.052 | °C/W |
| $R_{th(c-h)}$ | Thermal impedance (shell to powder) | 180° sine wave, single heat sink | | | 0.024 | °C/W |
| V_{iso} | Insulation voltage | | | | 2500 | V |
| F_M | Mounting force (M5) | | | | 12 | N-m |
| | Mounting force (M6) | | | | 6 | N-m |
| T_{stq} | Stored temperature | | | -40 | 125 | °C |
| W_t | Weight | | | | | g |
| Outline | | | | | | |

Peak On-state Voltage Vs. Peak On-state Current

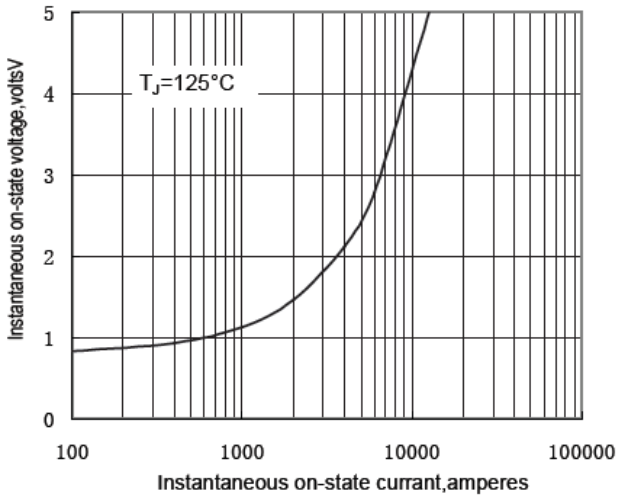


Fig.1

Max. junction To case Thermal Impedance Vs. Time

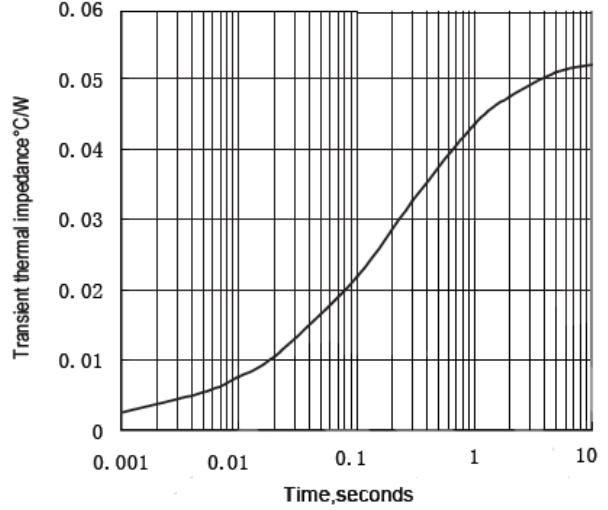


Fig.2

Max. Power Dissipation Vs. Mean On-state Current

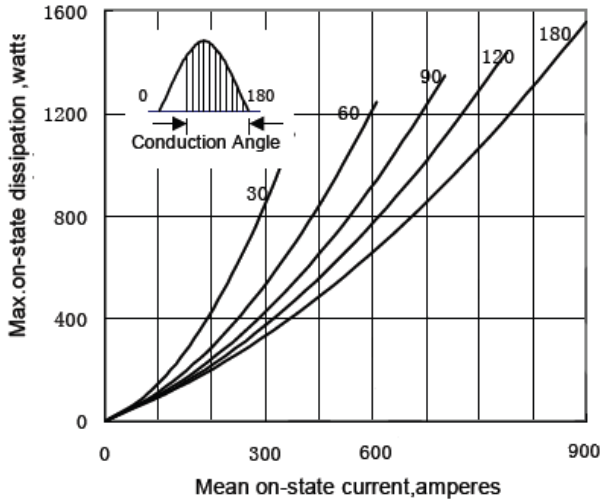


Fig.5

Max. heatsink Temperature Vs. Mean On-state Current

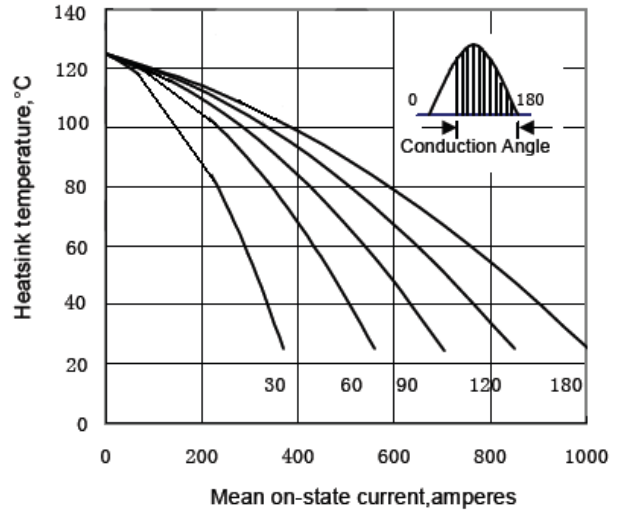


Fig.6

Max. Power Dissipation Vs. Mean On-state Current

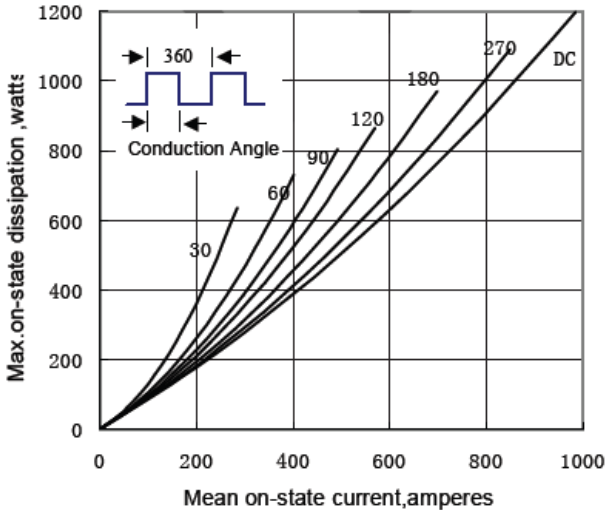


Fig.5

Max. case Temperature Vs. Mean On-state Current

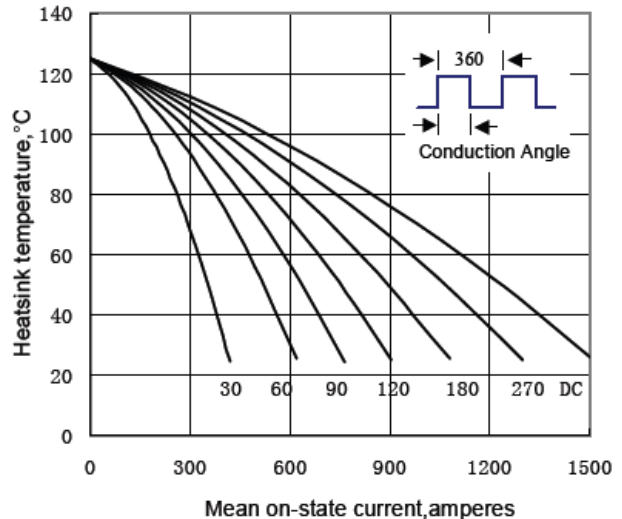


Fig.6

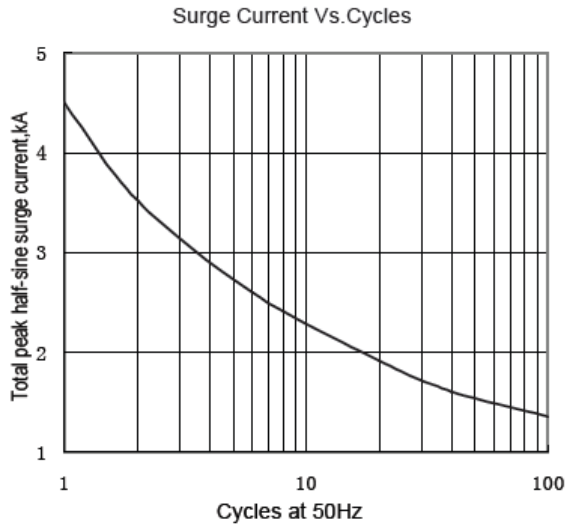


Fig.7

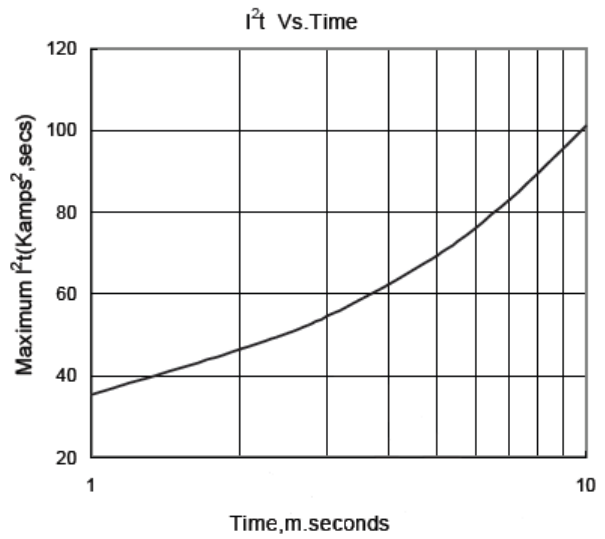


Fig.8

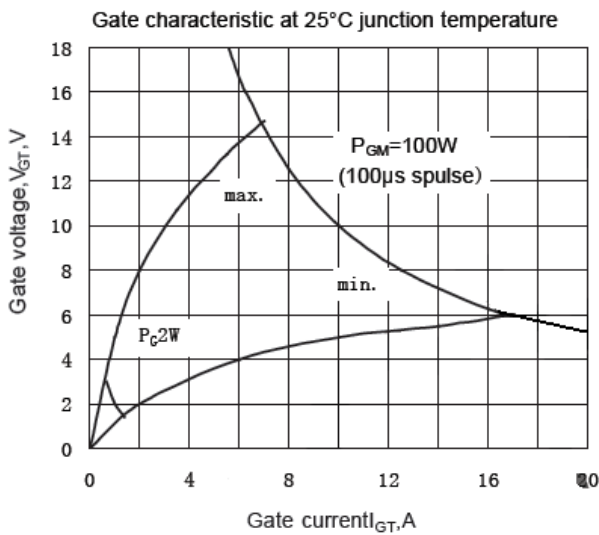


Fig.9

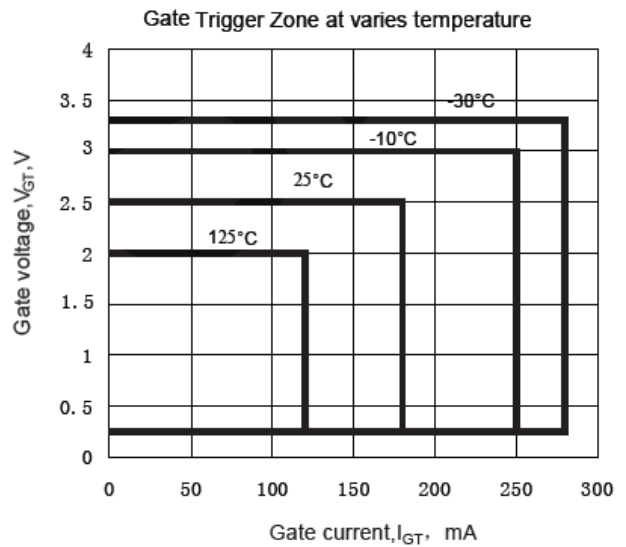
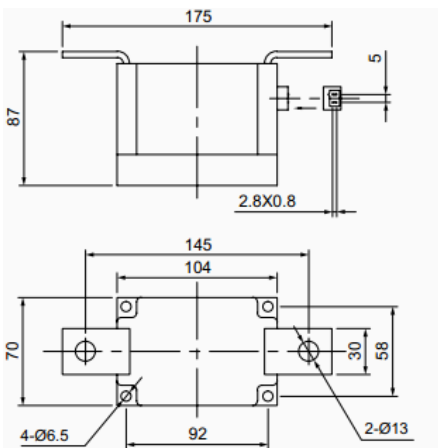


Fig.10

Outline:



1

Circuit Drawing:

